WHAT IS CLAIMED IS:

1. A process of forming a gate structure on a semiconductor substrate, comprising:

providing a semiconductor substrate having a channel region formed therein so as to define a source and a drain region and a gate structure comprised of a gate dielectric positioned on said channel region and a conductive layer positioned on said gate dielectric;

forming an insulator element region on said substrate; and

transforming a portion of said conductive layer adjacent said insulator element region into a sidewall spacer.

2. The process of Claim 1, wherein forming said insulator element region comprises doping said wafer with said insulator element.

3. The process of Claim 1, wherein said insulator element region comprises said insulator element and silicon.

4. The process of Claim 3, wherein said insulator element comprises nitrogen.

5. The process of Claim 4, wherein forming said insulator element region comprises doping the substrate with greater than about 10^{12} nitrogen atoms.

6. The process of Claim 1, wherein transforming said portion of said conductive layer comprises oxidizing said portion.

7. The process of Claim 6, wherein said conductive layer comprises polysilicon.

8. The process of Claim 6, wherein oxidizing said portion further comprises growing a bird's beak region extending laterally into a selected portion of said conductive layer.

9. The process of Claim 6, where oxidizing said portion further comprises forming a nitride layer on said semiconductor substrate.

10. The process of Claim 9, wherein said nitride layer laterally extends under at least a portion of said conductive layer.

11. The process of Claim 1, wherein said gate dielectric comprises silicon oxide.

12. The process of Claim 1, further comprising depositing a second sidewall spacer over the sidewall spacer.

13. A process of forming a gate structure on a semiconductor wafer comprising the steps of:

providing a semiconductor substrate having a channel region formed therein so as to define a source region and a drain region and a gate structure comprised of an isolation layer positioned on said channel region and a conductive layer positioned on said isolation layer;

implanting an insulator element into said source and drain regions;

oxidizing a portion of said conductive layer adjacent said implanted source and drain regions to form an oxide spacer and a protective layer over said source and drain regions, said protective layer comprising said insulator element and characterized by a dielectric constant higher than that of silicon oxide.

14. The process of Claim 13, wherein oxidizing said portion of said conductive layer comprises growing a bird's beak region extending laterally into a selected portion of said conductive layer and said protective layer extending at least partially under said conductive layer.

15. A process of forming a gate structure on a semiconductor wafer comprising the steps of:

providing a semiconductor wafer having a channel region formed therein so as to define a source and a drain region and a gate structure comprised of an isolation layer positioned over said channel region and a conductive layer positioned over said isolation layer;

implanting nitrogen into said source and drain regions;

transforming a portion of said conductive layer adjacent said insulator element region into an oxide spacer;

combining a portion of said substrate with said nitrogen to form a nitride protective layer over said substrate; and

depositing a sidewall spacer over the oxide spacer.

16. A semiconductor device comprising:

a substrate having a channel region interposed between a source and a drain region;

a gate structure comprised of an isolation layer positioned on said wafer adjacent said channel region and a conductive layer positioned on said isolation layer;

an insulating spacer over a portion of said conductive layer and extending in a gate bird's beak structure; and

a protective film having a higher dielectric constant than silicon oxide extending over said source and drain regions.

17. The semiconductor device in Claim 16, wherein said insulator film comprises an insulator element diffused from an insulator element region formed on said source and drain regions in said substrate.

18. The semiconductor device in Claim 17, wherein said insulator element region is formed by doping said source and drain regions by said insulator element.

19. The semiconductor device in Claim 17, wherein said insulator film is silicon nitride and said insulator element is nitrogen.

20. A semiconductor gate structure comprising:

a silicon channel;

a gate oxide positioned over said silicon channel;

a conductive gate electrode positioned over said gate oxide; and

a silicon nitride film extending at least partially over said silicon channel.

21. The gate structure of Claim 20, wherein the gate structure is a gate in a field effect transistor device.

22. The gate structure of Claim 20, further comprising an oxide spacer on a sidewall of said electrode and extending into a gate bird's beak structure under said electrode.

23. A process of eliminating hot electron injection into a gate electrode positioned on a gate oxide adjacent a channel interposed between a source and a drain region in a silicon substrate, the process comprising:

forming a nitrogen doped region in said source and drain regions; and

forming a silicon nitride film over a portion of said gate electrode so that a portion of said silicon nitride film penetrates under said gate electrode during said forming step wherein said portion of said silicon nitride film prevents hot electron injection into said gate electrode.

24. The process of Claim 23, wherein the step of forming silicon nitride film comprises exposing said gate electrode to an oxidizing ambient.

25. The process of Claim 23, further comprising double diffuse boron implanting said source and drain regions.

26. The process of Claim 23, further comprising:

depositing an insulating layer over said gate electrode; and

anisotropically etching said insulating layer to form sidewall spacers.

27. The process of Claim 24, further comprising source/drain implanting said source and drain regions.

28. The process of Claim 25, further comprising lightly doping said source and drain regions to grade a junction between said channel and said source and drain regions.